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| UNIVERSITY OF INFORMATION TECHNOLOGY  **COMPUTER ENGINEERING DEPARTMENT** | **FINAL EXAMINATION II (2019-2020)**  **COURSE: DEGITAL LOGIC DESIGN**  *Time duration: 70 minutes*  *(Paper materials are not allowed)*  *(OEP Students do the test by English,*  *Regular Students do the test by Vietnamese)* |

# Question 1: (5 points)

1. What is combinational circuit? Describe 5 combinational circuits
2. What is sequential circuit? Describe 5 sequential circuits
3. Describe 5 memory components
4. What is Register Transfer Logic (RTL) design?
5. How can we determine the operation frequency of a design circuit?
6. Compare the disadvantages and advantages between the single cycle design and the multiple cycle design?
7. What is the main purpose of a pipelined functional unit design?
8. What is the main purpose of a pipelined datapath design?
9. What is difference between register sharing technique and register merging technique?
10. What is difference between resource-constraint scheduling and time-constraint scheduling?

# Question 2: (2 points)

1. Show a Moore-based Finite-state machine (4 states) with datapath (FSDM) architecture of a system design.
2. Show a Mealy-based Finite-state machine (7 states) with datapath (FSDM) architecture of a system design.

# Question 3 (3 points)

Given: Sum =

1. Build the datapath to calculate the value of Sum.
2. Show the FSM graph to control the datapath built in (a).

**This examination’s learning outcomes (LO) (matching to subject syllabus’s LO)**

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| **Question** | **LO** | **Description** |
| 1 | G4 | Ability to comprehend professional materials |
| 2 | G1 | Ability to analyze finite state machine circuits, data paths, and control units*.* |
| 3 | G2 | Ability to design and optimize the circuits use ASM and FSMD models in the design process |

**Approved by Head of Subject Designed by**